

SC11100ZP
Patent application**IN THE CLAIMS**

Please cancel claim 3 without disclaimer or prejudice.

Please amend claims 1, 2, 16 and 19 by replacement with the following rewritten claims therefor, in accordance with 37 CFR § 1.121(c)(1)(i):

1. (twice amended) A method of manufacturing a semiconductor component comprising:

providing a substrate with a surface;

providing a layer comprising a thickness of at least six to approximately twelve nanometers of undoped gallium arsenide over the surface of the substrate;

forming a gate contact over a first portion of the layer; and

removing a second portion of the layer to expose a portion of the surface of the substrate, wherein the remaining first portion of said layer does not substantially extend beyond the horizontal profile of said gate contact.

2. (amended) The method of claim 1 wherein:

said layer comprises a thickness of at least six to approximately nine nanometers of undoped gallium arsenide.

16. (twice amended) A method of manufacturing a semiconductor component comprising:

providing a delta-doped, heteroepitaxial semiconductor substrate with a surface, the delta-doped, heteroepitaxial semiconductor substrate comprising:

a support layer comprised of semi-insulating gallium arsenide;

a buffer layer comprised of undoped gallium arsenide overlying the support layer;

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a doping layer delta-doped with silicon and overlying the buffer layer;

a spacer layer comprised of undoped gallium arsenide and overlying the doping layer;

a channel layer comprised of indium gallium arsenide and overlying the spacer layer; and

a barrier layer comprised of aluminum gallium arsenide and overlying the channel layer, the barrier layer forming the surface for the delta-doped, heteroepitaxial semiconductor substrate;

providing an undoped gallium arsenide capping layer having a thickness of at least six to approximately twelve nanometers and overlying the surface of the delta-doped, heteroepitaxial semiconductor substrate;

forming a gate contact over the undoped gallium arsenide capping layer, the gate contact covering a first portion of the undoped gallium arsenide capping layer and absent over a second portion of the undoped gallium arsenide capping layer;

removing the second portion of the undoped gallium arsenide capping layer after forming the gate contact to expose a portion of the surface of the delta-doped, heteroepitaxial semiconductor substrate, wherein the remaining first portion of said undoped gallium arsenide capping layer does not substantially extend beyond the horizontal profile of said gate contact;

forming a spacer adjacent to the gate contact;

forming source and drain regions in the delta-doped, heteroepitaxial semiconductor substrate; and

forming source and drain contacts over the source and drain regions after removing the second portion of the undoped gallium arsenide capping layer.

19. (amended) The method of claim 16 wherein: